Abstract of the Disclosure

A synchronous flash memory includes an array of non-volatile memory cells. The memory device has a package configuration that is compatible with an SDRAM. The memory device can comprise an array of memory cells having N addressable sectors, and control circuitry to control erase or write operations on the array of memory cells. Protection circuitry can be coupled to the control circuitry to selectively prevent erase or write operations from being performed on both first and last sectors of the N addressable sectors. The protection circuitry can comprise a multi-bit register having a first bit corresponding to the first sector and a second bit corresponding to the last sector.